CLAIMS

Please cancel claims without prejudice or disclaimer and please add new claims as shown in the following claim listing.

1-67. (Canceled).

68. (New) A method comprising:

identifying by an operating system entry of a processor into a C power state of an Advanced Configuration and Power Interface specification;

reading by the operating system a time corresponding to an exit of the processor from the C power state, wherein the processor exits from the C power state in response to an interrupt, wherein the processor executes an interrupt routine in response to the interrupt, and wherein the time corresponding to the exit is identified in response to the interrupt and prior to execution of the interrupt routine; and

determining by the operating system a duration corresponding to the C power state based on the time corresponding to the exit.

69. (New) The method of claim 68, wherein the C power state is a C1 power state.

70. (New) The method of claim 68, wherein the C power state is entered in response to a halt instruction.

71. (New) The method of claim 68, comprising:

causing by the operating system the time corresponding to the exit to be identified in response to the interrupt and prior to execution of the interrupt routine.

72. (New) The method of claim 68, comprising storing by the operating system the time corresponding to the exit in main memory.

73. (New) The method of claim 68, comprising storing by the operating system the time corresponding to the exit in the processor.

74. (New) The method of claim 68, comprising storing by the operating system the time corresponding to the exit in a chip.

75. (New) The method of claim 68, comprising storing by the operating system the time corresponding to the exit in a chipset.

76. (New) The method of claim 68, comprising identifying by the operating system a time corresponding to an entry of the processor into the C power state.

77. (New) The method of claim 76, comprising storing by the operating system the time corresponding to the entry in main memory.

78. (New) The method of claim 76, comprising storing by the operating system the time corresponding to the entry in the processor.

79. (New) The method of claim 76, comprising storing by the operating system the time corresponding to the entry in a chip.

80. (New) The method of claim 76, comprising storing by the operating system the time corresponding to the entry in a chipset.

81. (New) The method of claim 68, wherein the reading includes reading a counter.

82. (New) The method of claim 68, wherein the reading includes reading a counter in a chip.

83. (New) The method of claim 68, wherein the reading includes reading a counter in a chipset.

84. (New) The method of claim 68, comprising:

causing by the operating system a counter to be started in response to the identifying.

85. (New) The method of claim 68, comprising:

causing by the operating system a counter to be halted in response to the interrupt.

86. (New) The method of claim 68, comprising:

selecting by the operating system a C power state for the processor based on the determined duration.

87. (New) A method comprising:

identifying by an operating system entry of a processor into a C power state of an Advanced Configuration and Power Interface specification;

causing by the operating system a counter to be started;

identifying by the operating system an exit of the processor from the C power state in response to an interrupt;

causing by the operating system the counter to be halted; and

determining by the operating system a duration corresponding to the C power state based on a content of the counter.

88. (New) The method of claim 87, wherein the C power state is a C1 power state.

89. (New) The method of claim 87, wherein the C power state is entered in response to a halt instruction.

90. (New) The method of claim 87, wherein the processor executes an interrupt routine in response to the interrupt, and wherein the causing the counter to be halted is performed prior to execution of the interrupt routine.

91. (New) The method of claim 87, wherein the counter is in a chip.

92. (New) The method of claim 87, wherein the counter is in a chipset.

93. (New) The method of claim 87, comprising:

selecting by the operating system a C power state for the processor based on the determined duration.